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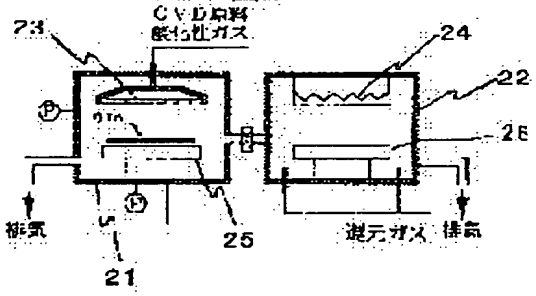
(54) MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE AND MANUFACTURING DEVICE THEREFOR

(57)Abstract:
PROBLEM TO BE SOLVED: To provide the manufacturing method of a semiconductor device in which a capacity is increased and a leakage current is suppressed by suppressing the generation of SiO2 on a boundary and removing impurity elements remaining in an insulation film, and to provide the manufacturing device.
SOLUTION: In the manufacturing method of the semiconductor device provided with the process of forming a gate insulation film on a silicon single crystal substrate, the process of forming the gate insulation film is provided with the process of forming an oxide layer by an organic metal gas and an oxidizing gas, and the process of heat-treating the oxide layer in a reducing atmosphere. Further, a semiconductor manufacturing device forms the gate insulation film.

図2



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The manufacturing method of the semiconductor device with which the process which forms said gate dielectric film on a silicon single crystal substrate in the manufacturing method of the semiconductor device which has the process which forms gate dielectric film is characterized by having the process which forms an oxide layer by organic metal gas and the oxidizing gas, and the process which heat-treats this oxide layer in reducing atmosphere.
[Claim 2] The process which forms an isolation insulator layer on a silicon single crystal substrate, and the process which forms gate dielectric film, The process which forms a gate electrode on this gate dielectric film, and the process which forms the source and a drain field in both sides on both sides of said gate dielectric film between said isolation insulator layers and said gate dielectric film, The process which forms the protective coat which protects said isolation insulator layer, gate dielectric film, gate electrode and source, and a drain field, In the manufacturing method of the semiconductor device which has the process which is made to penetrate said protective coat in contact with each of said source and a drain field, and forms a plug electrode, and the process which forms wiring on said protective coat in contact with this plug electrode one by one The manufacturing method of the semiconductor device with which the process which forms said gate dielectric film is characterized by having the process which forms an oxide layer by organic metal gas and the oxidizing gas, and the process which heat-treats this oxide layer in reducing atmosphere.
[Claim 3] The manufacture approach of a semiconductor device that said reducing atmosphere gas is characterized by being hydrogen or catalyst hydrogen in claim 1 or 2.
[Claim 4] The manufacture approach of the semiconductor device characterized by the heat treatment temperature in said reducing atmosphere gas being 500 degrees C or less in either of claims 1-3.
[Claim 5] The manufacture approach of the semiconductor device characterized by said gate dielectric film consisting of one or more kinds of TiO2, HfO2, ZrO2, aluminum 2O3, Ta2O5, Sc2O3, Y2O3, and Ln2O3 (Ln is rare earth elements) in either of claims 1-4.
[Claim 6] The manufacture approach of the semiconductor device characterized by dissolving said organic metal in a tetrahydrofuran, toluene, a hexane, an octane, and one or more sorts of solvents of alcohols, and forming said gate dielectric film in either of claims 1-6 by the liquid conveyance evaporation organic metal chemical-vapor-deposition method using the solution.
[Claim 7] It is. the manufacturing installation of the semiconductor device which forms gate dielectric film on a silicon single crystal substrate -- It has the heat treatment room which heat-treats said silicon single crystal substrate after forming the membrane formation room which forms the oxide layer used as said gate dielectric film on said silicon single crystal substrate, and said oxide layer in reducing atmosphere. The shower head with which said membrane formation room introduces organic metal gas and a oxidizing gas, It has evacuation equipment which exhausts the heater for substrate heating which lays and heats said silicon single crystal substrate, and said membrane formation room. Said heat treatment rooms are semiconductor fabrication machines and equipment characterized by having the heater for substrate heating which heats a reducing gas installation means to introduce said reducing gas, the evacuation

equipment which exhausts said heat treatment room, the base in which said silicon single crystal substrate is laid, and said substrate.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a new semiconductor device, the manufacture approach, and manufacturing installation of the MIS mold transistor component which has especially gate dielectric film with respect to the manufacturing installation.
[0002]
[Description of the Prior Art] In recent years, detailed-ization of an MIS (Metal Insulator Semiconductor) mold transistor component is in the situation which is at hand as Hasama even as for less than 0.1-micrometer gate length. such detailed-izing -- following -- as the ingredient of the gate dielectric film of an MIS transistor component -- specific inductive capacity -- SiO2 of 3.9 -- replacing -- aluminum2O of about 25 ZrO 2 and 10 -- using 3 or 80 TiO2 grades is examined. These ingredients can thicken physical thickness about 20 times 2.5 times about 6 times, in order to obtain the gate capacitance same since specific inductive capacity is high as SiO2. For this reason, also when a component is made detailed according to a scaling law, it is thought that the leakage current between the gate/substrate by the direct tunneling in gate dielectric film can be suppressed.
[0003] Although forming gate dielectric film by the spatter in the inside of an oxygen ambient atmosphere is shown in JP,8-51220,A, the specific process by organic metal gas is not indicated at all.
[0004]
[Problem(s) to be Solved by the Invention] however, MOCVD (Metalorganic Chemical Vapor Deposition) according these high dielectric materials to a usual organic metal raw material and oxygen reactant gas -- when it formed using law, it was easy to form SiO2 film of a low dielectric layer between Si single crystal and gate dielectric film with oxygen reactant gas, and there was surely a trouble of as a result falling the capacity of the whole gate dielectric film.
[0005] MOCVD according to a usual organic metal raw material and oxygen reactant gas in order to control formation of the above-mentioned low dielectric layer of SiO2 -- when it was going to control formation of SiO2 by carrying out the low dental-curing film using law, carbon and hydrogen which are contained in a raw material remained in the insulator layer mostly, and there was a problem from which lowering and the high dielectric constant of membraneous quality are hard to be obtained.
[0006] Furthermore, although it was heat-treating with the conventional technique after forming predetermined thickness, since carbon and hydrogen which remain in the film were emitted by heat treatment out of the film, the opening was generated, and there was a problem to which a membranous consistency falls. Moreover, for the reason, the problem to which the irregularity on the front face of gate dielectric film becomes large was also produced.
[0007] The object of this invention controls the generation of SiO2 by the interface, and is by removing the impurity element which remains in an insulator layer to offer the manufacture approach and manufacturing installation of the semiconductor device which is high capacity and suppressed leakage current.

[0008]
[Means for Solving the Problem] This invention is characterized by having the process in which the process which forms said gate dielectric film on a silicon single crystal substrate in the manufacturing method of the semiconductor device which has the process which forms gate dielectric film forms an oxide layer by organic metal gas and the oxidizing gas, and the process which heat-treats this oxide layer in reducing atmosphere.
[0009] Moreover, the process at which this invention more specifically forms an isolation insulator layer on a silicon single crystal substrate, The process which forms gate dielectric film, and the process which forms a gate electrode on this gate dielectric film, The process which forms the source and a drain field in both sides on both sides of said gate dielectric film between said isolation insulator layers and said gate dielectric film, The process which forms the protective coat which protects said isolation insulator layer, gate dielectric film, gate electrode and source, and a drain field, In the manufacturing method of the semiconductor device which has the process which is made to penetrate said protective coat in contact with each of said source and a drain field, and forms a plug electrode, and the process which forms wiring on said protective coat in contact with this plug electrode one by one The process which forms said gate dielectric film is characterized by having the process which forms an oxide layer by organic metal gas and the oxidizing gas, and the process which heat-treats this oxide layer in reducing atmosphere.
[0010] Said gate dielectric film consists [that said reducing atmosphere gas is hydrogen or catalyst hydrogen,] of one or more kinds of TiO2, HfO2, ZrO2, aluminum 2O3, Ta2O5, Sc2O3, Y2O3, and Ln2O3 (Ln is rare earth elements), It is desirable to dissolve said organic metal in a tetrahydrofuran, toluene, a hexane, an octane, and one or more sorts of solvents of alcohols, and to form said gate dielectric film by the liquid conveyance evaporation organic metal chemical-vapor-deposition method using the solution.
[0011] That is, the description of this invention is in the MIS (MetalInsulator Semiconductor) mold transistor component which used the silicon single crystal substrate as the base material to perform the process which forms gate dielectric film at low temperature using a CVD raw material and oxygen gas, and the process in reducing atmosphere gas to heat-treat by turns.
[0012] According to this invention, formation of SiO2 can be controlled to Si single crystal and a gate-dielectric-film interface by forming membranes at low temperature first. As for whenever [substrate stoving temperature / when forming gate dielectric film], it is desirable to carry out at 300 degrees C - 400 degrees C.
[0013] Next, it is possible to remove the carbon which remained in the film by heat treatment by reducing atmosphere gas, and hydrogen. 500 degrees C or less of things for which an impurity is removed efficiently are preferably possible for the heat treatment temperature at this time by carrying out at 400-500 degrees C. If it carries out at temperature higher than 500 degrees C, the reduction reaction of gate dielectric film will arise and lowering of a withstand voltage property will arise. Moreover, at temperature lower than 400 degrees C, if rapid temperature-up heating is used in reducing atmosphere heat treatment, the thing whose a possibility that an impurity element may remain in gate dielectric film, and decline in a dielectric constant may arise is and which an impurity removes still more effectively will become possible again. This invention can obtain the MIS mold transistor component which is high capacity and suppressed leakage current by controlling the generation of SiO2 by the interface, and removing an impurity by performing the above-mentioned membrane formation and reduction processing mutually.
[0014] It is. the manufacturing installation of the semiconductor device with which this invention forms gate dielectric film on a silicon single crystal substrate -- It has the heat treatment room which heat-treats said silicon single crystal substrate after forming the membrane formation room which forms the oxide layer used as said gate dielectric film on said silicon single crystal substrate, and said oxide layer in reducing atmosphere. The shower head with which said membrane formation room introduces organic metal gas and a oxidizing gas, It has evacuation equipment which exhausts the heater for substrate heating which lays and heats said silicon single crystal substrate, and said membrane formation room. Said heat treatment room is characterized by having the heater for substrate heating which heats a reducing gas installation

means to introduce said reducing gas, the evacuation equipment which exhausts said heat treatment room, the base in which said silicon single crystal substrate is laid, and said substrate.
[0015]
[Embodiment of the Invention] (Example 1) The process of this invention is shown in drawing 1 . this invention -- MOCVD (Metalorganic Chemical Vapor Deposition) -- membranes are formed using law and, subsequently it heat-treats by reducing atmosphere gas. This membrane formation and heat treatment are repeatedly performed so that it may become predetermined thickness, and it is characterized by producing gate dielectric film.
[0016] Drawing 2 is the sectional view of the semiconductor fabrication machines and equipment which form the gate dielectric film concerning this invention. In this invention, it has the heat treatment room 22 for considering reducing atmosphere heat treatment as the membrane formation room 21 for forming gate dielectric film. It conveys in the heat treatment room 22 after forming gate dielectric film at the membrane formation room 21, and heat treatment in reducing atmosphere is performed. In addition, the configuration of equipment may be changed and membrane formation and reducing atmosphere heat treatment may be performed by turns at a membrane formation room.
[0017] The semiconductor fabrication machines and equipment which form the gate dielectric film concerning this invention have the lamp for substrate heating which heats the base 26 and the substrate which lay a reducing gas installation means to by_which have evacuation equipment which exhausts the heater 25 for substrate heating and the membrane-formation room 21 which lay and heat the shower head 23 and the silicon single crystal substrate with which the membrane-formation room 21 introduces organic metal gas and a oxidizing gas, and a heat treatment room 22 introduces reducing gas, the evacuation equipment which exhaust a heat treatment room 22, and a silicon single crystal substrate.
[0018] Si single crystal substrate is a substrate of field (100) bearing, resistivity 10 - 15 ohm-cm in p-type. After forming a slot with a depth of about 0.4 micrometers for a component isolation region, CVD-SiO2 film was formed completely, and next, by CMP, said substrate was made to carry out flattening and it produced to it.
[0019] Next, in order to produce ZrO2 film used as gate dielectric film, Zr(t-OC4H9) 4 (Tetratertiarybutoxy zirconium) organic metal was prepared by the concentration of 0.05-0.25 mols/l. to the solvent of C4H8O (tetrahydrofuran), and it considered as the CVD raw material. The CVD raw material was supplied at the rate of 0.1 - 3sccm using the liquid massflow controller. After setting the temperature of a carburetor as 100-200 degrees C and making a CVD raw material into gas from a liquid at a stretch, it conveyed by Ar gas 198 - 500sccm. Next, it introduced into the reaction container, after mixing a CVD raw material / Ar gas, oxygen reactant gas 2 - 800sccm. The pressure of a reaction container was set to 0.01 - 50torr, and membrane formation temperature was formed on 350-degree C conditions.
[0020] Next, reducing atmosphere heat treatment was performed for said gate dielectric film using hydrogen gas. Heat treatment conditions are rapid temperature up for 10 minutes at 450 degrees C.
[0021] On the heat-treated gate dielectric film, ZrO2 film was formed by the above-mentioned membrane formation approach like the process shown in drawing 1 , said reducing atmosphere heat treatment was repeated and ZrO2 film of 20nm of deed thickness was formed.
[0022] As a comparison, the above-mentioned membrane formation approach was used on said substrate, ZrO2 film of 20nm of thickness was formed, and ZrO2 film heat-treated in the hydrogen ambient atmosphere was produced. The impurity analysis result in the film is shown in drawing 3 . This invention was decreasing from the sample for a comparison as substantially [the impurity in the film] as 1/10 or less. Moreover, as a result of observing a cross section, by this invention, eburnation of the sample for a comparison was carried out to many openings having been observed into ZrO2 film.
[0023] Next, 300nm of polycrystal Si film used as a gate electrode was formed, Lynn was poured into the n channel field and boron was poured into the p channel field, respectively, and it heat-treated among the nitrogen-gas-atmosphere mind of 800 degrees C and 10 - 30min, and was activated. The gate electrode carried out patterning of the polycrystal Si film using the usual

phot lithography method, and in the self aryne, it was etched by RIE and it formed it. Moreover, gate dielectric film processed and formed ZrO2 similarly. Next, the mask of the gate electrode was carried out, the ion implantation of the atom (P, As, Sb) the periodic table's 5th group's or the 3rd group's atom (B, aluminum, Ga, In) was performed to the source / drain field, and the diffusion region of low resistance was formed by performing 800 degrees C and heat treatment of 30sec among Ar. Next, SiO2 protective coat was formed with the CVD method.

[0024] After producing a through hole on the source/drain furthermore, W-plug electrode was produced with the CVD method. Finally aluminum wiring was produced on W-plug and the MIS mold transistor component was produced. aluminum wiring of one of the two was carried out to the ground, and EOT (SiO2 conversion thickness) was computed from the C-V property at the time of making it change to a gate electrode -2-2V. The result is shown in drawing 4 . The inclination searched for from the least square method of ZrO2 data between 10-30nm thickness meant the dielectric constant, and was about 20. moreover, ZrO2 and Si single crystal substrate interface which are gate dielectric film from EOT showing abbreviation zero when physical thickness is zero — low — it turns out that SiO two-layer dielectric constant formation has been controlled. As an example of a comparison, the sample which heat-treated ZrO2 after 20nm membrane formation was processed like the above. The result of this ZrO2 film is shown in drawing 4 . The dielectric constant for which it asked from the inclination of data was about 20, and EOT in physical thickness zero was about 2.0nm. these 2.0nm — low — forming in ZrO2 and Si single crystal substrate interface whose SiO2 dielectric constant film is gate dielectric film is shown.

[0025] In this example, although carried out using hydrogen gas as reducing atmosphere gas, even if it uses catalyst hydrogen, the same effectiveness is acquired.

[0026] Moreover, although ZrO2 was used as gate dielectric film in this example, the dielectric materials which consist of one or more kinds of TiO2, HfO2, ZrO2, aluminum 2O3, Ta2O5, Sc2O3, Y2O3, and Ln2O3 (Ln:La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu) can be manufactured similarly. Moreover, although Polycrystal Si is used as a gate electrode, the above-mentioned dielectric materials and the metal which does not react, for example, W, Mo, and TiN, and TiSi2 grade may be used. Furthermore, Lynn may be doped to Polycrystal Si. although aluminum wiring was explained — low — it is easy to be a metallic material [****], for example, Cu ingredient may be used.

[0027] In this example, by combining the process which forms gate dielectric film at low temperature using CVD material gas and oxygen gas, and the heat treatment process in reducing atmosphere gas, the impurity element which remains in an insulator layer can be removed, and the semiconductor device which can, as a result, control high-capacity-izing of gate dielectric film, generating of leak, etc. can be offered. Since it can produce without as a result reducing the capacity of the whole gate dielectric film, the MIS transistor component which sets the gate die length to 0.1 micrometers or less can be manufactured.

[0028]

[Effect of the Invention] Above, according to this invention, SiO2 film formation of a low dielectric layer could be controlled between Si single crystal and gate dielectric film by combining a CVD raw material, the process which forms membranes using oxygen gas, and the process in reducing atmosphere gas to heat-treat, and it became possible to produce the semiconductor device which has precise gate dielectric film which does not have an impurity further.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the manufacture process of the gate dielectric film concerning this invention.
[Drawing 2] It is the sectional view of the membrane formation equipment of the gate dielectric film concerning this invention.
[Drawing 3] It is drawing [the example of a comparison / amount / of impurities / in the film of this invention].
[Drawing 4] It is the diagram showing the relation between the ZrO2 physics thickness of this invention, and EOT thickness.
[Description of Notations]
21 [— The lamp for heating, 25 / — The heater for substrate heating, 26 / — Cradle.] — A membrane formation room, 22 — A heat treatment room, 23 — The shower head, 24

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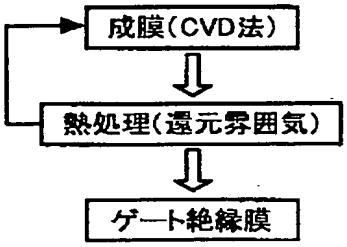
DRAWINGS

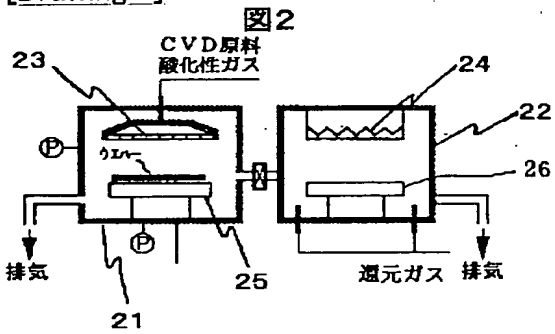
[Drawing 1]

図1



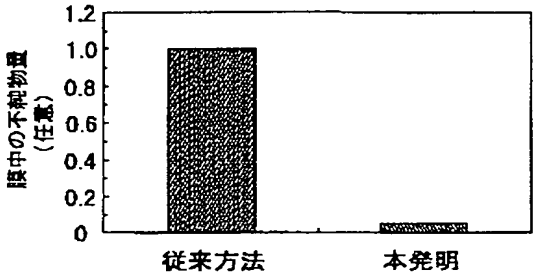
[Drawing 2]

図2



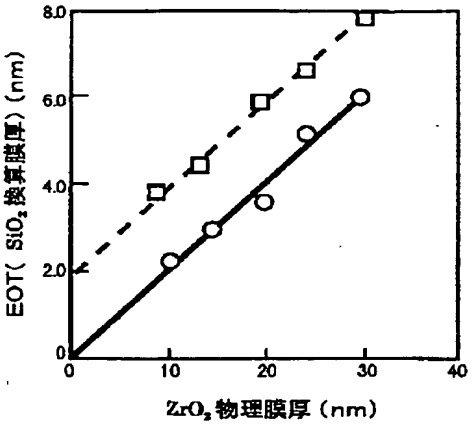
[Drawing 3]

図3



[Drawing 4]

図4



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特開２００３－１７６８４

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最終頁に続く

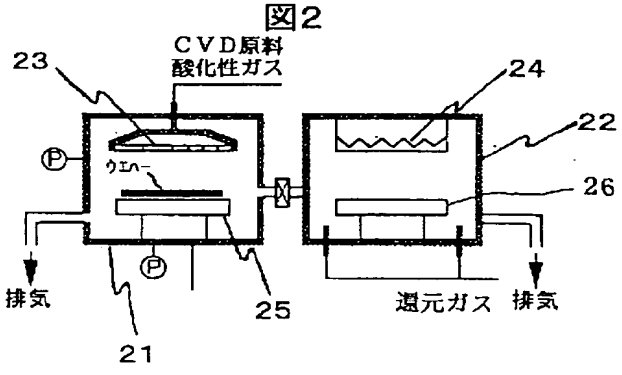
(54)【発明の名称】半導体装置の製造方法とその製造装置

(57)【要約】

【課題】本発明の目的は、界面でのSiO_2の生成を抑制し、絶縁膜中に残留する不純物元素を除去することにより高容量でかつリーク電流を抑えた半導体装置の製造方法とその製造装置を提供することにある。

【解決手段】本発明は、シリコン単結晶基板上に、ゲート絶縁膜を形成する工程を有する半導体装置の製造法において、前記ゲート絶縁膜を形成する工程が、有機金属ガスと酸化性ガスとによって酸化物層を形成する工程と、該酸化物層を還元雰囲気中で熱処理する工程とを有することを特徴とし、更にゲート絶縁膜を形成する半導体製造装置にある。

図2



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【特許請求の範囲】

【請求項１】シリコン単結晶基板上に、ゲート絶縁膜を形成する工程を有する半導体装置の製造法において、前記ゲート絶縁膜を形成する工程が、有機金属ガスと酸化性ガスとによって酸化物層を形成する工程と、該酸化物層を還元雰囲気中で熱処理する工程とを有することを特徴とする半導体装置の製造法。

【請求項２】シリコン単結晶基板上に、素子分離絶縁膜を形成する工程と、ゲート絶縁膜を形成する工程と、該ゲート絶縁膜上にゲート電極を形成する工程と、前記素子分離絶縁膜と前記ゲート絶縁膜との間で前記ゲート絶縁膜を挟んで両側にソース及びドレイン領域を形成する工程と、前記素子分離絶縁膜とゲート絶縁膜とゲート電極とソース及びドレイン領域とを保護する保護膜を形成する工程と、前記ソース及びドレイン領域の各々に接して前記保護膜を貫通させてプラグ電極を形成する工程と、該プラグ電極に接して前記保護膜上に配線を形成する工程とを順次有する半導体装置の製造法において、前記ゲート絶縁膜を形成する工程が、有機金属ガスと酸化性ガスとによって酸化物層を形成する工程と、該酸化物層を還元雰囲気中で熱処理する工程とを有することを特徴とする半導体装置の製造法。

【請求項３】請求項１又は２において、前記還元雰囲気ガスが、水素又は触媒水素であることを特徴とする半導体装置の製造方法。

【請求項４】請求項１～３のいずれかにおいて、前記還元雰囲気ガスでの熱処理温度が５００℃以下であることを特徴とする半導体装置の製造方法。

【請求項５】請求項１～４のいずれかにおいて、前記ゲート絶縁膜がTiO_2，HfO_2，ZrO_2，Al_2O_3，Ta_2O_5，Sc_2O_3，Y_2O_3，Ln_2O_3（Ｌｎは希土類元素）の１種類以上からなることを特徴とする半導体装置の製造方法。

【請求項６】請求項１～６のいずれかにおいて、前記有機金属をテトラヒドロフラン、トルエン、ヘキサン、オクタン及びアルコール類の１種以上の溶剤に溶解し、その溶液を用いる液体搬送気化有機金属化学気相成長法によって前記ゲート絶縁膜を形成することを特徴とする半導体装置の製造方法。

【請求項７】シリコン単結晶基板上に、ゲート絶縁膜を形成する半導体装置の製造装置おいて、前記シリコン単結晶基板上に前記ゲート絶縁膜となる酸化物層を形成する成膜室と前記酸化物層を形成後の前記シリコン単結晶基板を還元雰囲気中で熱処理する熱処理室とを備え、前記成膜室は有機金属ガスと酸化性ガスとを導入するシャワーヘッド、前記シリコン単結晶基板を載置し加熱する基板加熱用ヒータ及び前記成膜室を排気する真空排気装置を有し、前記熱処理室は前記還元ガスを導入する還元ガス導入手段、前記熱処理室を排気する真空排気装置、前記シリコン単結晶基板を載置する台及び前記基板を加熱する基板加熱用ヒータ、を有することを特徴とする半導体製造装置。

2

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、新規な半導体装置の製造方法とその製造装置に係わり、特にゲート絶縁膜を有するＭＩＳ型トランジスタ素子の製造方法とその製造装置に関する。

【０００２】

【従来の技術】近年、ＭＩＳ（Ｍｅｔａｌ Ｉｎｓｕｌａｔｏｒ Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）型トランジスタ素子の微細化は０．１μｍ未満のゲート長まで目前に迫っている状況である。このような微細化に伴ってＭＩＳトランジスタ素子のゲート絶縁膜の材料として、比誘電率が３．９のSiO_2に代って約２５のZrO_2、１０のAl_2O_3、８０のTiO_2等を用いることが検討されている。これらの材料は比誘電率が高いためにSiO_2と同一のゲート容量を得るために物理膜厚を約６倍、２．５倍、２０倍程度厚くすることができる。このためにスケーリング則に従って素子を微細化した場合にも、ゲート絶縁膜中の直接トンネリングによるゲート／基板間のリーク電流を抑えられると考えられる。

【０００３】特開平８－５１２２０号公報には、酸素雰囲気中でのスパッタ法によってゲート絶縁膜を形成することが示されているが、有機金属ガスによる特定の製法は全く開示されていない。

【０００４】

【発明が解決しようとする課題】ところが、これらの高誘電体材料を通常の有機金属原料と酸素反応ガスによるＭＯＣＶＤ（Ｍｅｔａｌｏｒｇａｎｉｃ Ｃｈｅｍｉｃａｌ Ｖａｐｏｒ Ｄｅｐｏｓｉｔｉｏｎ）法を用いて形成した場合に、どうしても酸素反応ガスによってＳｉ単結晶とゲート絶縁膜の間に低誘電体層のSiO_2膜を形成しやすく、その結果ゲート絶縁膜全体の容量を低下する問題点があった。

【０００５】上記低誘電体層のSiO_2の形成を抑制するために、通常の有機金属原料と酸素反応ガスによるＭＯＣＶＤ法を用いて、低温成膜することによりＳｉＯ２の形成を抑制しようとすると、原料に含まれる炭素や水素が多く絶縁膜中に残留し、膜質の低下や高い誘電率が得られにくい問題があった。

【０００６】更に従来技術では、所定の膜厚を成膜後に熱処理を行なっているが、膜中に残留する炭素や水素が熱処理により膜外に放出されるため空隙が生じ、膜の密度が低下する問題があった。また、そのため、ゲート絶縁膜表面の凹凸が大きくなる問題も生じた。

【０００７】本発明の目的は、界面でのSiO_2の生成を抑制し、絶縁膜中に残留する不純物元素を除去することにより高容量でかつリーク電流を抑えた半導体装置の製造方法とその製造装置を提供することにある。

【０００８】

【課題を解決するための手段】本発明は、シリコン単結晶基板上に、ゲート絶縁膜を形成する工程を有する半導体装置の製造法において、前記ゲート絶縁膜を形成する工程が、有機金属ガスと酸化性ガスとによって酸化物層を形成する工程と、該酸化物層を還元雰囲気中で熱処理する工程とを有することを特徴とする。

【０００９】又、本発明は、より具体的には、シリコン単結晶基板上に、素子分離絶縁膜を形成する工程と、ゲート絶縁膜を形成する工程と、該ゲート絶縁膜上にゲート電極を形成する工程と、前記素子分離絶縁膜と前記ゲート絶縁膜との間で前記ゲート絶縁膜を挟んで両側にソース及びドレイン領域を形成する工程と、前記素子分離絶縁膜とゲート絶縁膜とゲート電極とソース及びドレイン領域とを保護する保護膜を形成する工程と、前記ソース及びドレイン領域の各々に接して前記保護膜を貫通させてプラグ電極を形成する工程と、該プラグ電極に接して前記保護膜上に配線を形成する工程とを順次有する半導体装置の製造法において、前記ゲート絶縁膜を形成する工程が、有機金属ガスと酸化性ガスとによって酸化物層を形成する工程と、該酸化物層を還元雰囲気中で熱処理する工程とを有することを特徴とする。

【００１０】前記還元雰囲気ガスが、水素又は触媒水素であること、前記ゲート絶縁膜がTiO_2，HfO_2，ZrO_2，Al_2O_3，Ta_2O_5，Sc_2O_3，Y_2O_3，Ln_2O_3（Lnは希土類元素）の１種類以上からなること、前記有機金属をテトラヒドロフラン、トルエン、ヘキサン、オクタン及びアルコール類の１種以上の溶剤に溶解し、その溶液を用いる液体搬送気化有機金属化学気相成長法によって前記ゲート絶縁膜を形成することが好ましい。

【００１１】即ち、本発明の特徴は、シリコン単結晶基板を母材としたＭＩＳ（Ｍｅｔａｌ Ｉｎｓｕｌａｔｏｒ Ｓｅｍｉｃｏｎｄｕｃｔｏｒ）型トランジスタ素子において、ゲート絶縁膜をＣＶＤ原料と酸素ガスを利用して低温で成膜する工程と還元雰囲気ガスでの熱処理する工程を交互に行なうことにある。

【００１２】本発明によれば、まず低温で成膜することによりＳｉ単結晶とゲート絶縁膜界面にSiO_2の形成を抑制することができる。ゲート絶縁膜を成膜する時の基板加熱温度は、３００℃～４００℃で行なうのが好ましい。

【００１３】次に、還元雰囲気ガスでの熱処理により膜中に残留した炭素や水素を除去することが可能である。この時の熱処理温度は、５００℃以下、好ましくは４００～５００℃で行なうことにより、効率良く不純物を除去することが可能である。５００℃より高い温度で行なうと、ゲート絶縁膜の還元反応が生じて耐電圧特性の低下が生じる。また４００℃より低い温度では、不純物元素がゲート絶縁膜中に残留し誘電率の低下が生じる恐れ

があるまた、還元雰囲気熱処理において、急速昇温加熱を用いるとより、さらに効果的に不純物が除去することが可能となる。本発明は、上記成膜と還元処理を相互に行なうことにより、界面でのSiO_2の生成を抑制し、かつ不純物を除去することにより高容量でかつリーク電流を抑えたＭＩＳ型トランジスタ素子を得ることができる。

【００１４】本発明は、シリコン単結晶基板上に、ゲート絶縁膜を形成する半導体装置の製造装置おいて、前記シリコン単結晶基板上に前記ゲート絶縁膜となる酸化物層を形成する成膜室と前記酸化物層を形成後の前記シリコン単結晶基板を還元雰囲気中で熱処理する熱処理室とを備え、前記成膜室は有機金属ガスと酸化性ガスとを導入するシャワーヘッド、前記シリコン単結晶基板を載置し加熱する基板加熱用ヒータ及び前記成膜室を排気する真空排気装置を有し、前記熱処理室は前記還元ガスを導入する還元ガス導入手段、前記熱処理室を排気する真空排気装置、前記シリコン単結晶基板を載置する台及び前記基板を加熱する基板加熱用ヒータ、を有することを特徴とする。

【００１５】

【発明の実施の形態】（実施例１）図１に本発明のプロセスを示す。本発明では、ＭＯＣＶＤ（Ｍｅｔａｌ ｏｒｇａｎｉｃ Ｃｈｅｍｉｃａｌ Ｖａｐｏｒ Ｄｅｐｏｓｉｔｉｏｎ）法を用いて成膜し、次いで還元雰囲気ガスで熱処理を行う。この成膜と熱処理を所定の膜厚になるように繰り返し行い、ゲート絶縁膜を作製することを特徴とする。

【００１６】図２は、本発明に係るゲート絶縁膜を形成する半導体製造装置の断面図である。本発明では、ゲート絶縁膜を成膜する為の成膜室２１と還元雰囲気熱処理をする為の熱処理室２２を備えたものである。成膜室２１にてゲート絶縁膜を成膜後、熱処理室２２に搬送し、還元雰囲気中での熱処理を行なう。尚、装置の構成を変えて、成膜室で成膜と還元雰囲気熱処理を交互に行なっても良い。

【００１７】本発明に係るゲート絶縁膜を形成する半導体製造装置は、成膜室２１が有機金属ガスと酸化性ガスとを導入するシャワーヘッド２３、シリコン単結晶基板を載置し加熱する基板加熱用ヒータ２５及び成膜室２１を排気する真空排気装置を有し、又、熱処理室２２が還元ガスを導入する還元ガス導入手段、熱処理室２２を排気する真空排気装置、シリコン単結晶基板を載置する台２６及び基板を加熱する基板加熱用ランプを有する。

【００１８】Ｓｉ単結晶基板は、ｐ－ｔｙｐｅで（１００）面方位、抵抗率１０～１５Ω・ｃｍの基板である。前記基板に、素子分離領域を深さ約０．４μｍの溝を形成した後にＣＶＤ－SiO_2膜を全面成膜し、次にＣＭＰで平坦化させて作製した。

【００１９】次にゲート絶縁膜となるＺｒＯ２膜を作製

するために、Ｚｒ（ｔ－ＯＣ４Ｈ９）４（Ｔｅｔｒａｔｅｒｔｉａｒｙｂｕｔｏｘｙ ｚｉｒｃｏｎｉｕｍ）有機金属をＣ４Ｈ８Ｏ（テトラヒドロフラン）の溶剤に０．０５～０．２５ｍｏｌ／ｌの濃度で調合してＣＶＤ原料とした。ＣＶＤ原料は液体マスフローコントローラーを用いて０．１～３ｓｃｃｍの速度で供給した。気化器の温度を１００～２００℃に設定してＣＶＤ原料を一気に液体からガスにした後、Ａｒガス１９８～５００ｓｃｃｍで搬送した。次にＣＶＤ原料／Ａｒガスと酸素反応ガス２～８００ｓｃｃｍを混合した後、反応容器に導入した。反応容器の圧力を０．０１～５０ｔｏｒｒとし、成膜温度を３５０℃の条件で成膜した。

【００２０】次に、前記ゲート絶縁膜を水素ガスを用いて還元雰囲気熱処理を行った。熱処理条件は、-４５０℃で１０分間、急速昇温である。

【００２１】熱処理したゲート絶縁膜上に、図１に示す工程のように上記成膜方法でZrO_2膜を成膜し、前記還元雰囲気熱処理を繰り返し行い膜厚２０ｎｍのZrO_2膜を成膜した。

【００２２】比較として、前記基板上に上記成膜方法を用いて膜厚２０ｎｍのZrO_2膜を成膜し、水素雰囲気中で熱処理したZrO_2膜を作製した。図３に膜中の不純物分析結果を示す。本発明は比較用試料より、膜中の不純物が1/１０以下と大幅に減少していた。また、断面を観察した結果、比較用試料は、ZrO_2膜中に空隙が多数観察されたのに対して、本発明では、緻密化していた。

【００２３】次にゲート電極となる多結晶Ｓｉ膜を３００ｎｍ成膜し、ｎチャンネル領域にはリンを、ｐチャンネル領域にはボロンをそれぞれ注入し、８００℃、１０～３０ｍｉｎの窒素雰囲気中熱処理して活性化した。ゲート電極は多結晶Ｓｉ膜を通常のホトリソグラフィー法を用いてパターニングし、セルフアラインにてＲＩＥによりエッチングして形成した。また同様にゲート絶縁膜もZrO_2を加工して形成した。次にゲート電極をマスクしてソース/ドレイン領域に周期率表の第５族の原子（Ｐ，Ａｓ，Ｓｂ）或いは第３族の原子（Ｂ，Ａｌ，Ｇａ，Ｉｎ）のイオン注入を行い、８００℃、３０ｓｅｃのＡｒ中熱処理を施す事により低抵抗の拡散域を形成した。次にＣＶＤ法によりSiO_2保護膜を形成した。

【００２４】さらにソース/ドレイン上にスルーホールを作製した後、ＣＶＤ法によりＷ－プラグ電極を作製した。最後にＡｌ配線をＷ－プラグ上に作製してＭＩＳ型トランジスタ素子を作製した。片方のＡｌ配線をアースにして、ゲート電極に－２～２Ｖ変化させた場合のＣ－Ｖ特性よりＥＯＴ（SiO_2換算膜厚）を算出した。その結果を図４に示す。１０～３０ｎｍ膜厚間でZrO_2データの最小２乗法から求めた勾配は誘電率を意味し、約２０であった。また物理膜厚がゼロの場合にＥＯＴが約ゼロを示す事より、ゲート絶縁膜であるZrO_2とＳｉ単結晶基板界面に低誘電率なSiO_2層の形成を抑制できたことが分かる。比較例として、ZrO_2を２０ｎｍ成膜後に熱処理した試料を、上記と同様に加工した。このZrO_2膜の結果を図４に示す。データの勾配から求めた誘電率は約２０であり、物理膜厚ゼロにおけるＥＯＴが約２．０ｎｍであった。この２．０ｎｍは低誘電率なSiO_2膜がゲート絶縁膜であるZrO_2とＳｉ単結晶基板界面に形成していることを示している。

【００２５】本実施例では、還元雰囲気ガスとして水素ガスを用いて行なったが、触媒水素を用いても同様の効果が得られる。

【００２６】また、本実施例ではゲート絶縁膜としてZrO_2を用いたが、TiO_2，HfO_2，ZrO_2，Al_2O_3，Ta_2O_5，Sc_2O_3，Y_2O_3，Ln_2O_3（Ｌｎ：Ｌａ，Ｃｅ，Ｐｒ，Ｎｄ，Ｐｍ，Ｓｍ，Ｅｕ，Ｇｄ，Ｔｂ，Ｄｙ，Ｈｏ，Ｅｒ，Ｔｍ，Ｙｂ，Ｌｕ）の１種類以上からなる誘電体材料でも同様に製造可能である。またゲート電極として多結晶Ｓｉを用いているが、上記誘電体材料と反応しない金属、例えばＷ，Ｍｏ，ＴｉＮ，ＴｉＳｉ２等を用いてもよい。さらに、多結晶Ｓｉにリンをドープしてもよい。Ａｌ配線を説明したが、低抵抗な金属材料ならよく、例えばＣｕ材料を用いてもよい。

【００２７】本実施例においては、ゲート絶縁膜を、ＣＶＤ原料ガスと酸素ガスを利用して低温で成膜する工程と還元雰囲気ガスでの熱処理工程を組み合わせることにより、絶縁膜中に残留する不純物元素を除去し、その結果ゲート絶縁膜の高容量化とリークの発生等を抑制できる半導体装置を提供することができるものである。その結果ゲート絶縁膜全体の容量を低下させることなく作製できるために、そのゲート長さを０．１μｍ以下とするＭＩＳトランジスタ素子を製造できる。

【００２８】

【発明の効果】以上本発明によれば、ＣＶＤ原料と酸素ガスを利用して成膜する工程と還元雰囲気ガスでの熱処理する工程を組み合わせることで、Ｓｉ単結晶とゲート絶縁膜の間に低誘電体層のＳｉＯ２膜形成を抑制でき、さらに不純物の無い緻密なゲート絶縁膜を有する半導体装置を作製することが可能となった。

【図面の簡単な説明】

【図１】　本発明に係るゲート絶縁膜の製造プロセスを示すブロック図である。

【図２】　本発明に係るゲート絶縁膜の成膜装置の断面図である。

【図３】　本発明の膜中の不純物量を比較例と比較した図である。

【図４】　本発明のZrO_2物理膜厚とＥＯＴ膜厚との関係を示す線図である。

【符号の説明】

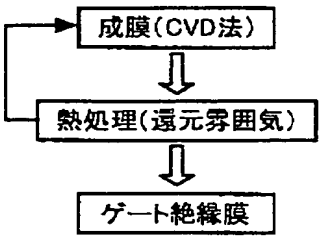
２１…成膜室、２２…熱処理室、２３…シャワーヘッ

7　　8

ド、２４…加熱用ランプ、２５…基板加熱用ヒータ、２６…受台。

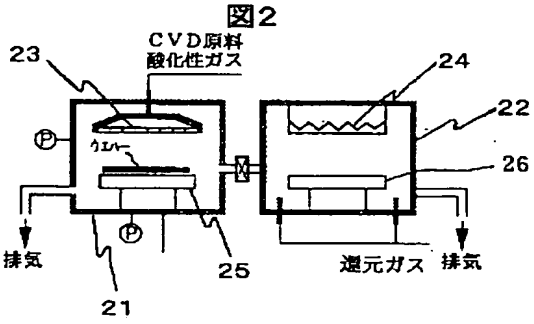
【図１】

図1



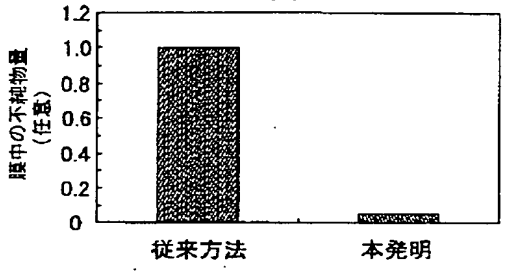
【図２】

図2



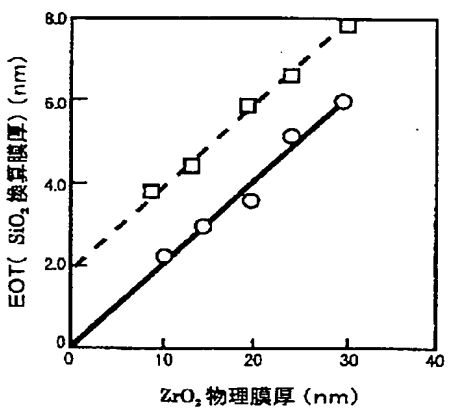
【図３】

図3



【図４】

図4



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